STRUCTURES AND METHODS FOR SELECTIVELY APPLYING A WELL BIAS TO PORTIONS OF A PROGRAMMABLE DEVICE

ABSTRACT

Structures and methods for selectively applying a well bias to only those portions of a PLD where such a bias is necessary or desirable, e.g., applying a positive well bias to transistors on critical paths within a user's design. A substrate for an integrated circuit includes a plurality of wells, each of which can be independently and programmably biased with the same or a different well bias voltage. In one embodiment, FPGA implementation software automatically determines the critical paths and generates a configuration bitstream that enables positive well biasing only for the transistors participating in the critical paths, or only for programmable logic elements (e.g., CLBs or lookup tables) containing those transistors. In another embodiment, negative well biasing is selectively applied to reduce leakage current.